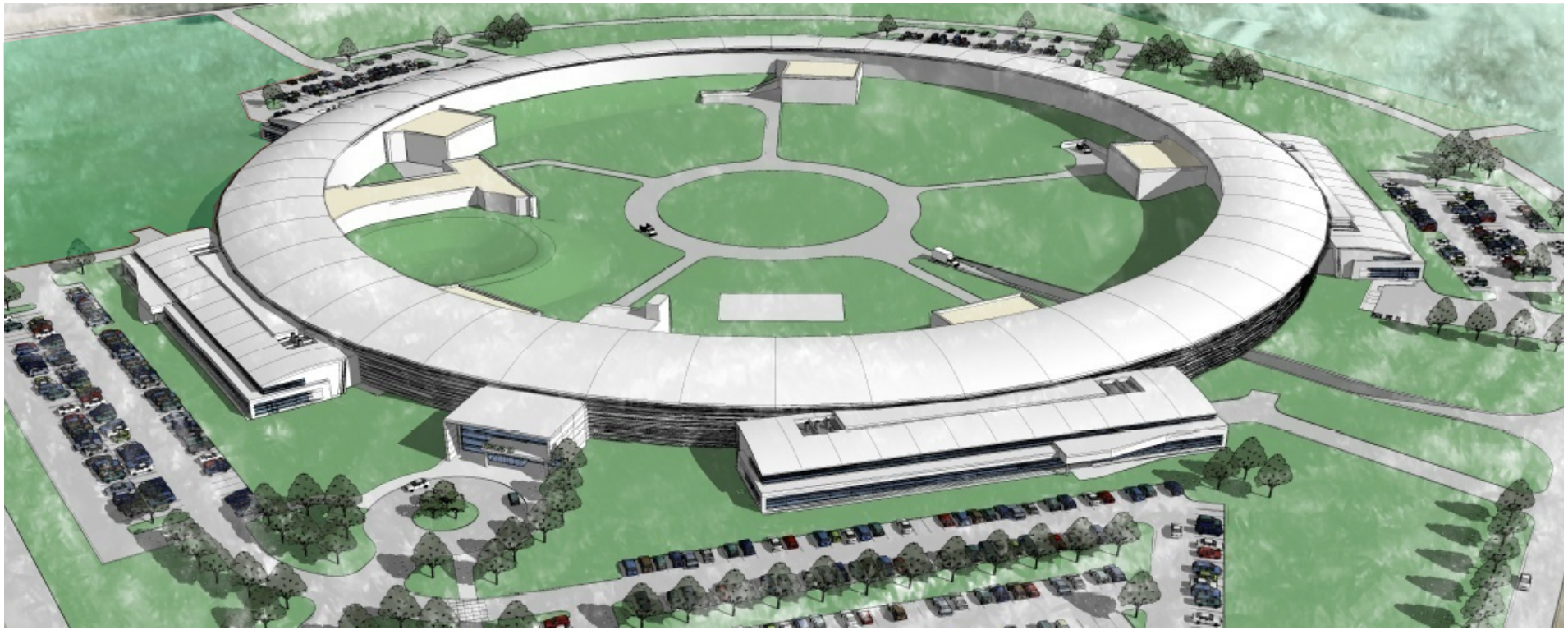
NSLS-II Sub-Micron RF BPM Development Update



February 18, 2011
Kurt Vetter
On Behalf of the "NSLS-II RF BPM Development Team"

Office of Science
U.S. DEPARTMENT OF ENERGY

BROOKHAVEN NATIONAL LABORATORY
BROOKHAVEN SCIENCE ASSOCIATES

Outline

- Introduction
- System Architecture Overview
- Beam Test Results
- Long-Term Stability Test Results

NSLS-II RF BPM Development Team

B. Bacha (Technical Support)

A. DellaPenna - (AFE, RF)

J. DeLong – (Timing, SDI Link)

K. Ha - (Embedded Processing, FPGA Architecture Controls)

B. Kosciuk - (Mechanical)

M. Maggipinto – (Technical Support)

J. Mead – (DFE, DSP, FPGA Architecture)

S. Orban – (Chassis Development)

I. Pinayev – (Physics)

G.Portman – Collaborator (ALS)

J.Sebek – Collaborator (SLAC)

Y. Tian – (FPGA, controls)

K. Vetter – Team Leader

BOLD – indicates Full-Time

Introduction

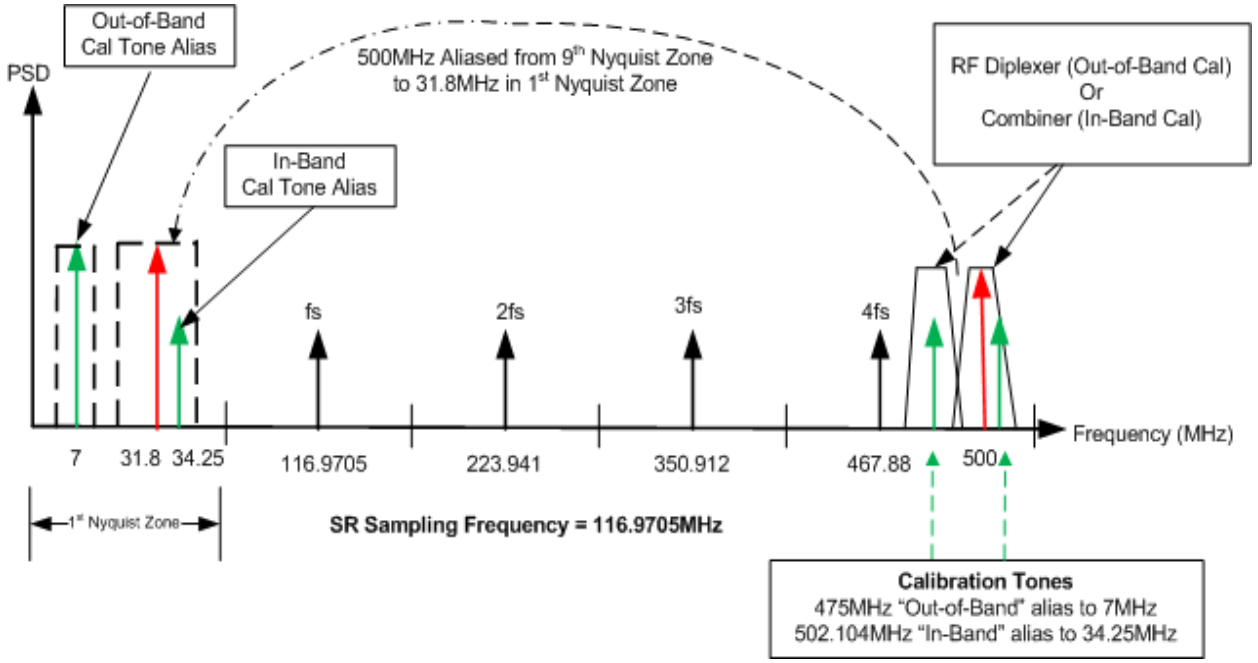
- Motivation – Why design our own BPM?
  - Technology → Use latest technology for World Class Synchrotron
  - System Architecture → Create generic architecture
  - In-House Expertise → Expertise resides in-house for all system aspects
  - Cost → Reduce re-occurring cost by ~50%
- Design Decisions
  - Build two separate boards → AFE and DFE
  - Partition boards at ADC output → AFE includes ADC's
  - Use Soft-Core Microprocessor → Design Portability
  - TCP/IP Interface → Direct EPICS and Matlab communication
  - No Fan → Leverage NSLS-II thermally stable racks, +/- 0.1°C, increase reliability
  - Long-Term Stability → Combination of stable thermal rack and Pilot-Tone
- Challenges
  - Schedule: start 8/2009, Booster production start 6/2010, SR production start 9/2011
  - 200nm resolution, 200nm 8hr stability

System Features

Data Type	Mode	Max Length	Description
ADC	On-Demand	1 Million samples each channel simultaneously	Raw ADC data (117Mhz sample rate)
TbT	On-Demand	1 Million Turns (X, Y, Sum, Q)	Turn-by-Turn data (Sample rate = Frev)
FA	On-Demand	1 Million (X, Y, Sum, Q)	Fast Acquisition Data (10KHz sample rate)
SA	Streaming	N/A (X, Y, Sum, Q)	Slow Acquisition Data (10Hz sample rate) Stream data over SDI link from FPGA Fabric
System Health	On-Demand	N/A	Xilinx Die Temperature DFE Board Temperature AFE Board Temperature SDI Link Communication Test Packets

- Embedded EventLink Receiver
- Front Panel External Trigger Inputs (2)
- Front Panel External Outputs (s)
- Rear Panel Machine Clock input (phase synchronization)

System Architecture Overview



The ADC clock is phase-locked to the Booster machine clock via an external machine clock reference supplied by the timing system. The PLL multiplies the Booster machine clock by 62 to achieve a sampling frequency of 117.3491MHz. The sub-sampled 499.68MHz RF fundamental signal is translated to a digital IF frequency of 30.28MHz (i.e. 16th harmonic of Booster revolution frequency).

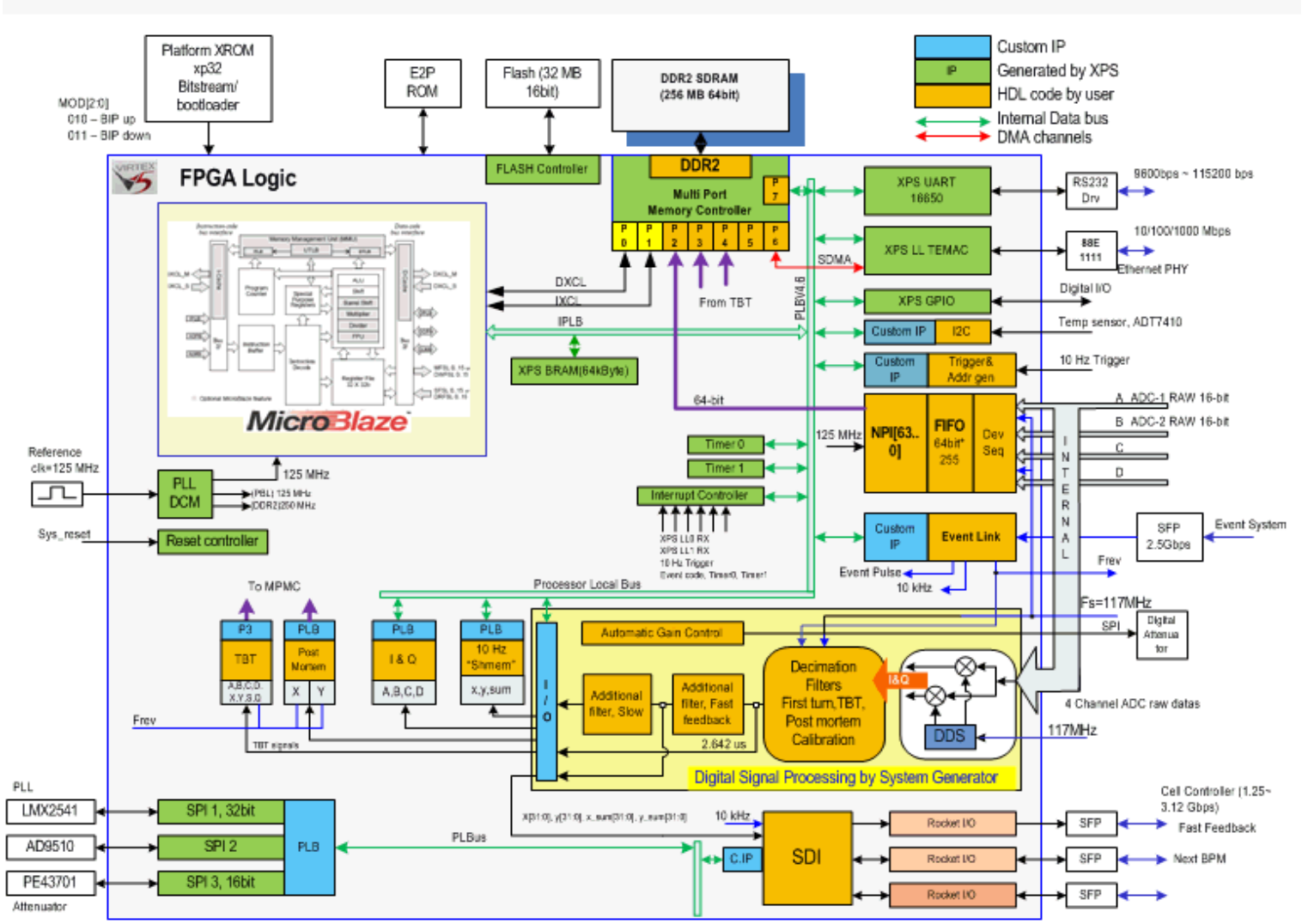
Booster ADC Clock Synthesizer							
Parameter	Booster	Units	Min	Max	Change	Centroid	Tunning Range (+/- ppm), min
RF Frequency	499.6800	MHz	499.6510	499.7090	0.0580		
Harmonic	264						
Frev Multiplication (Samples-per-turn)	62						
Revolution Frequency	**1.8927**	**MHz**	**1.892617**	**1.892837**	**0.0002**		
ADC Clock	**117.3491**	**MHz**	**117.3423**	**117.3559**	**0.0136**	**117.3491**	**59**
4*Fs	**469.3964**						
DDC Harmonic	**16**						
FA Decimation	190						
FA Output Frequency	9.9617	KHz	9.9611	9.9623	0.0012		
SA Decimation	262144						
SA Output Frequency	7.2202	Hz	7.2198	7.2206	0.0008		
Digital IF Frequency	**30.28187879**	Hz					

Booster Numerology

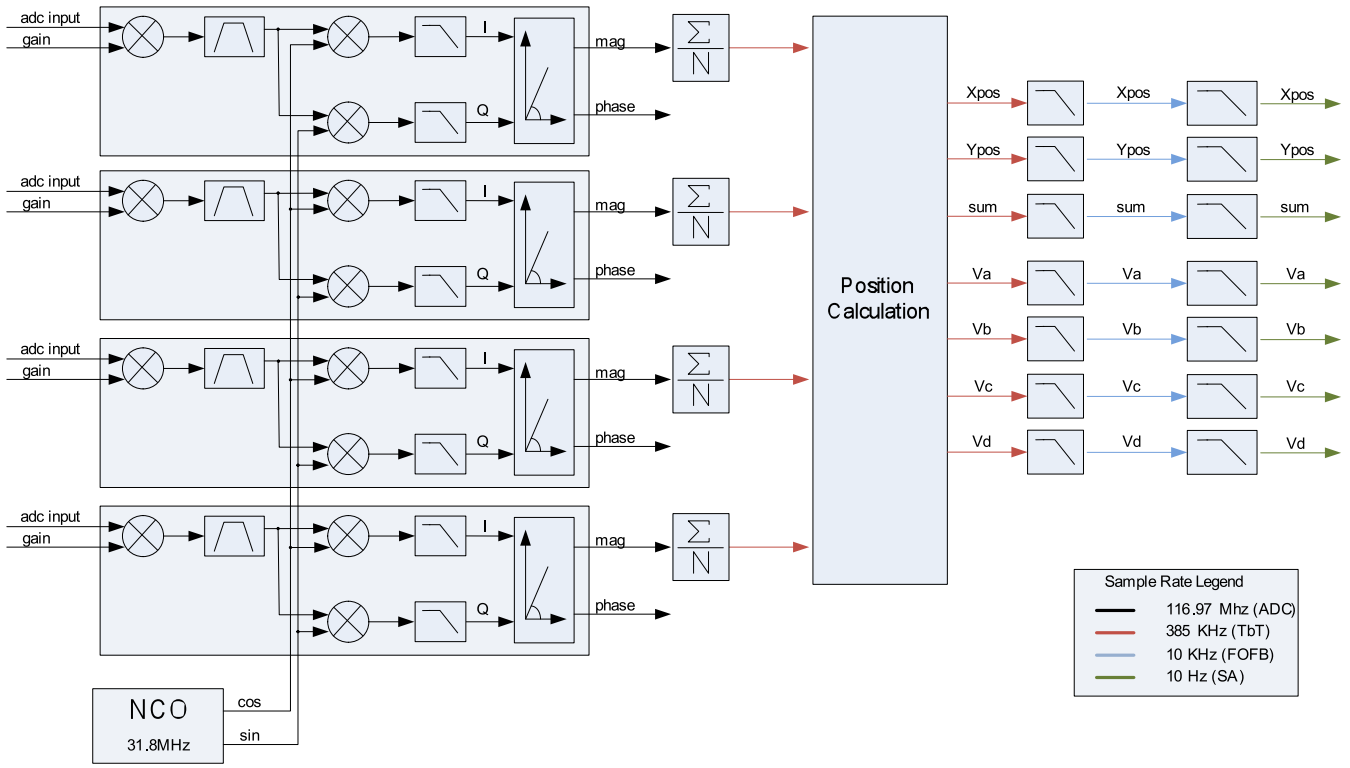
SR Scales by 5x

- Frev =1.8927MHz/5
- 310 samples per Turn
- DDC Harmonic = 80

System Architecture – DFE FPGA

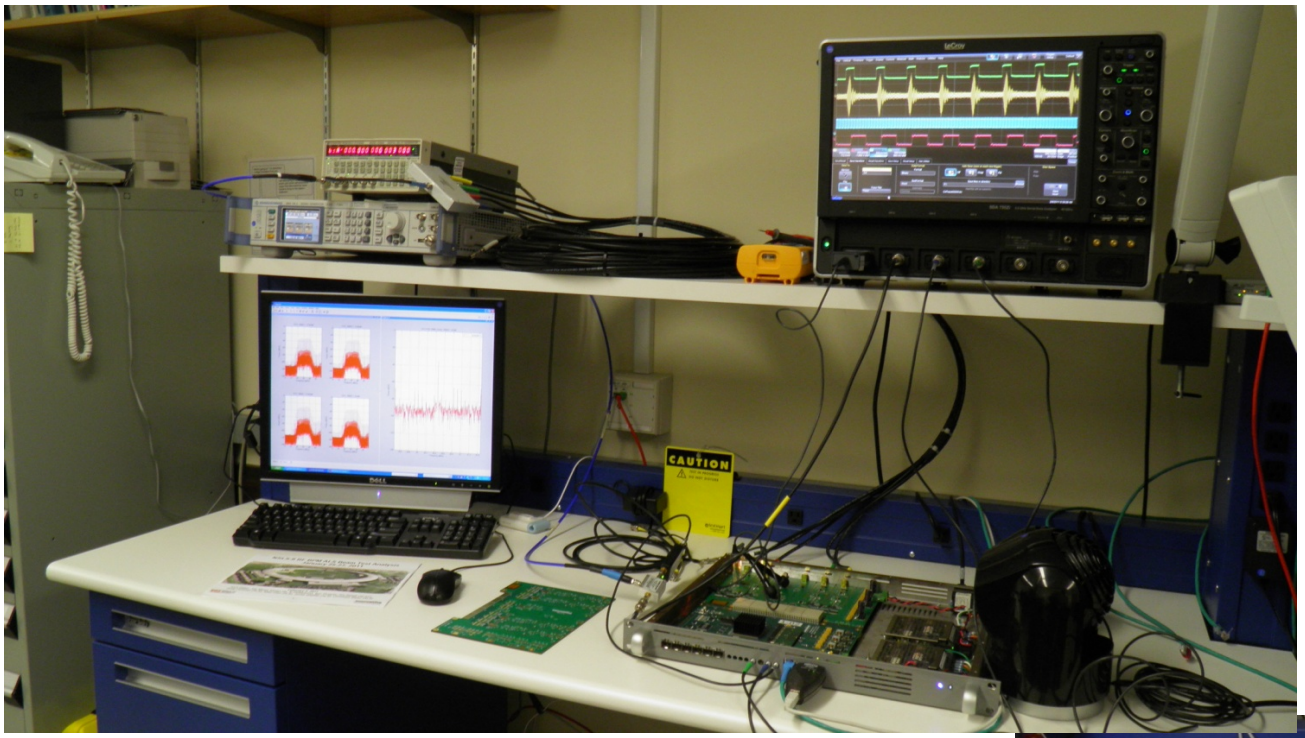


System Architecture – DFE DSP



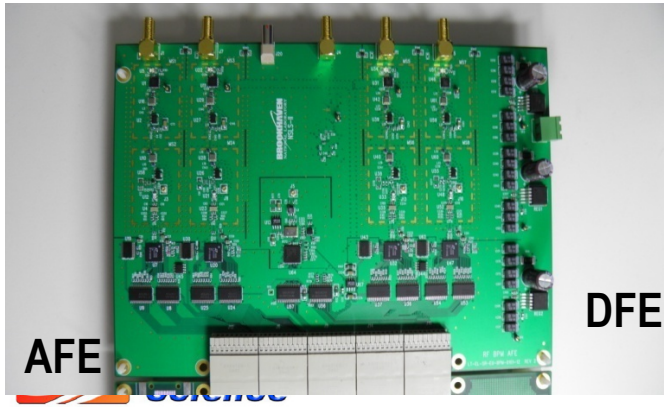
The digital signal processing chain consists of four identical channels. Each channel contains a digital down-converter, which is then followed by a programmable length averager which sums the magnitude outputs over a single turn. The position is then calculated, which is followed by additional filtering and decimation.

BPM Laboratory Testing



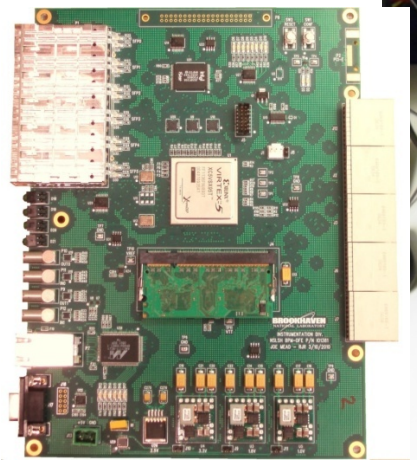
Test setup simulating ALS synchronous single-bunch measurements

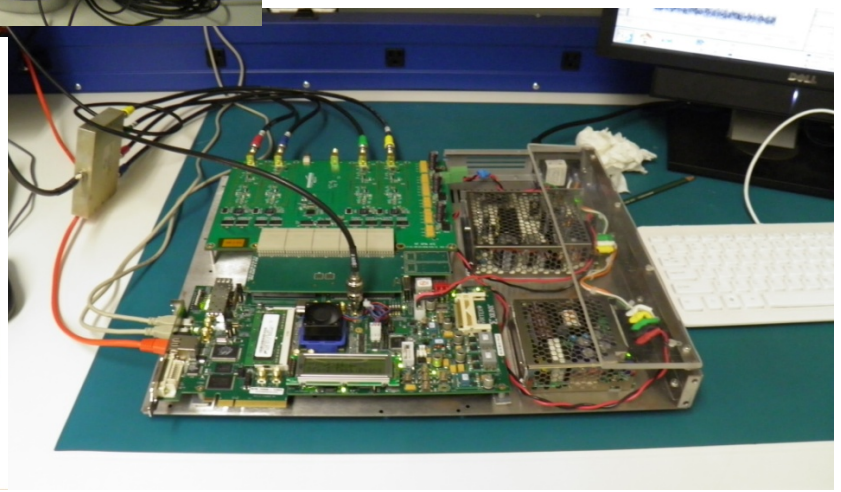
Virtex-6 Transitional development platform using ML605



AFE

DFE

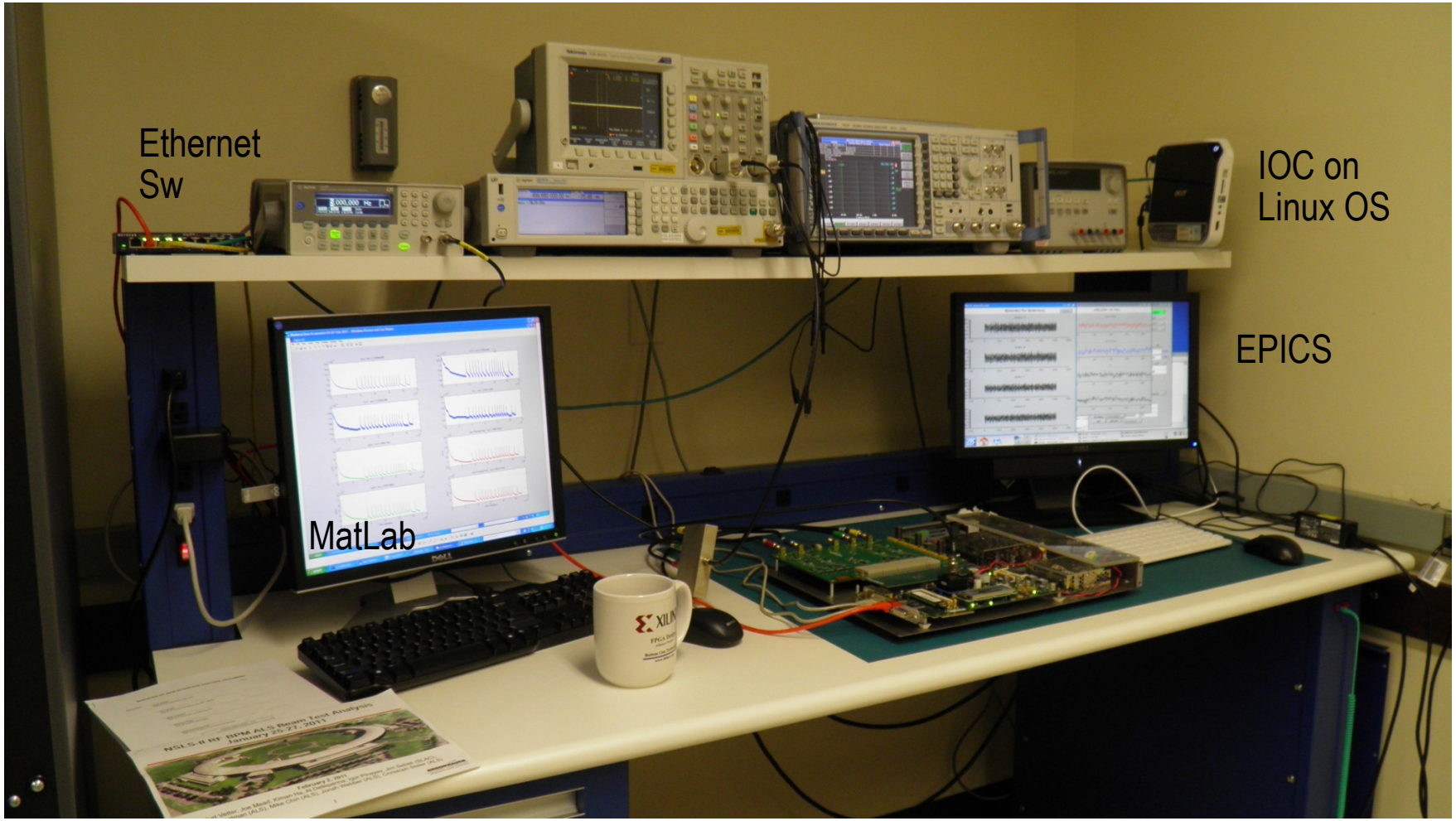




U.S. DEPARTMENT OF ENERGY

BPM Virtex-6 Transitional Platform

EPICS and Matlab Connectivity via TCP/IP

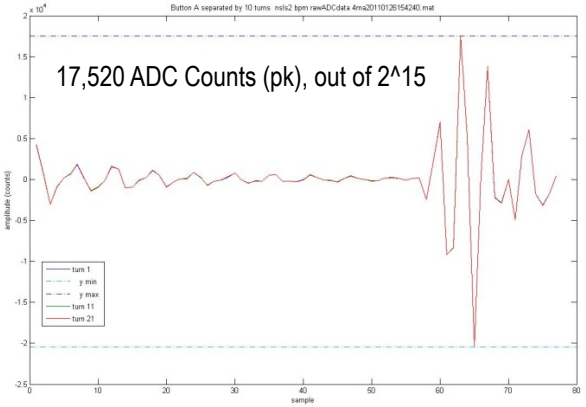


ALS Beam Test Results

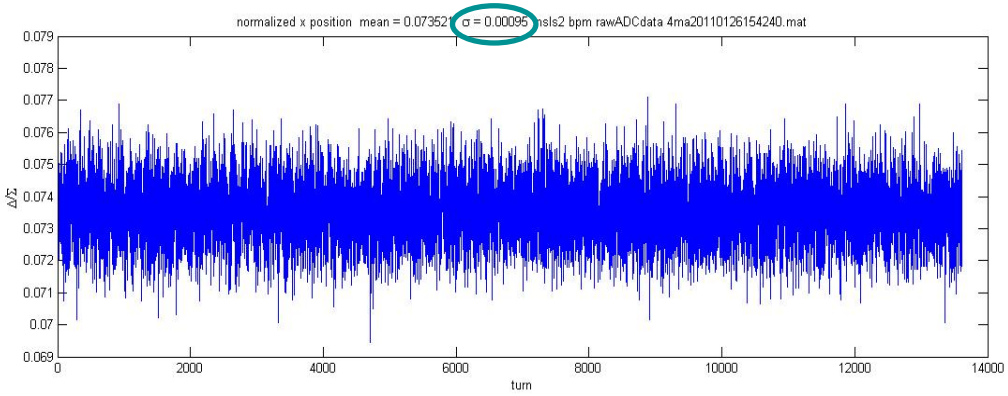
- Single-Bunch, Single-Pass
- Multi-Bunch Turn-By-Turn
- FOFB

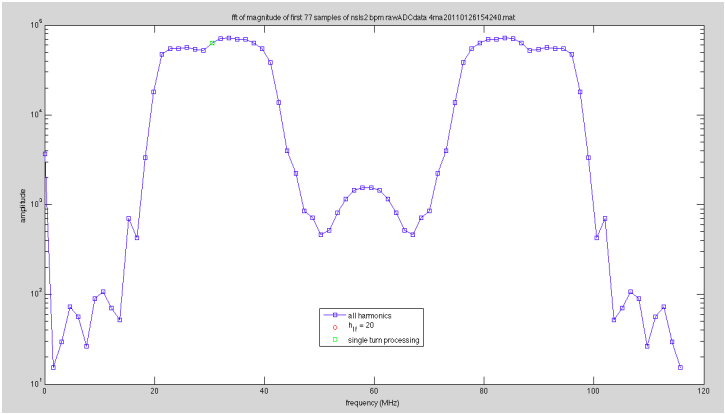
ALS Single-Bunch Performance

4ma (2.6nC) Single Bunch – 77 Samples/Turn @ Trev=656ns

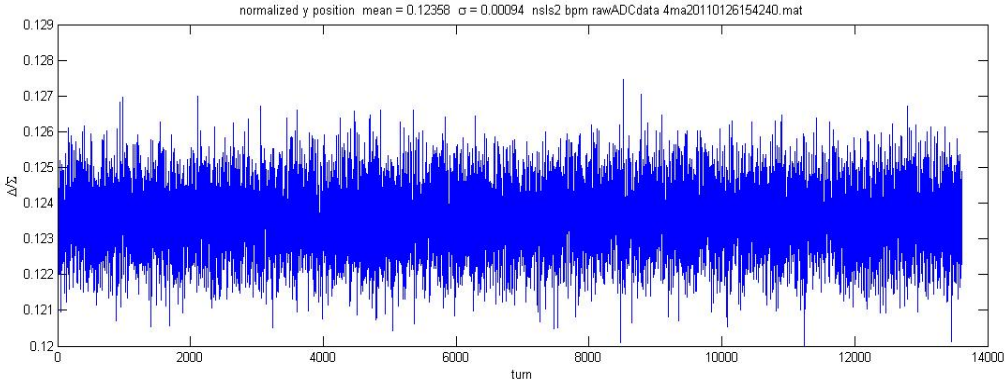


Overlay of Turns 1,11, and 21





FFT of first 77-samples (1-turn) Process h=20

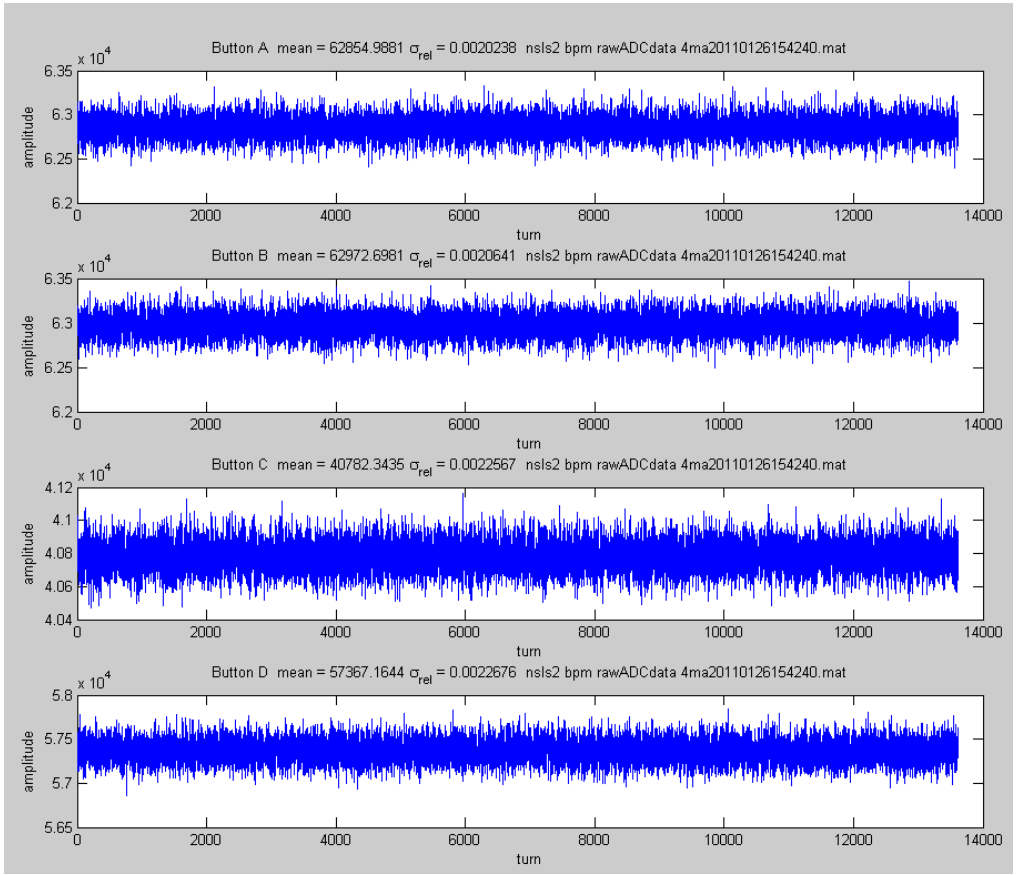


Normalized response yields approximate spatial resolution of 1-part in a 1,000. This measurement includes 10dB of insertion loss between BPM pickup and BPM electronics (6dB pad on button, 3dB for Pilot-Tone combiner, 1dB for 9m of ¼" heliax). Removing the 10dB loss would yield a normalized spatial resolution of = 0.000314 or approximately 0.3-parts per 1,000.

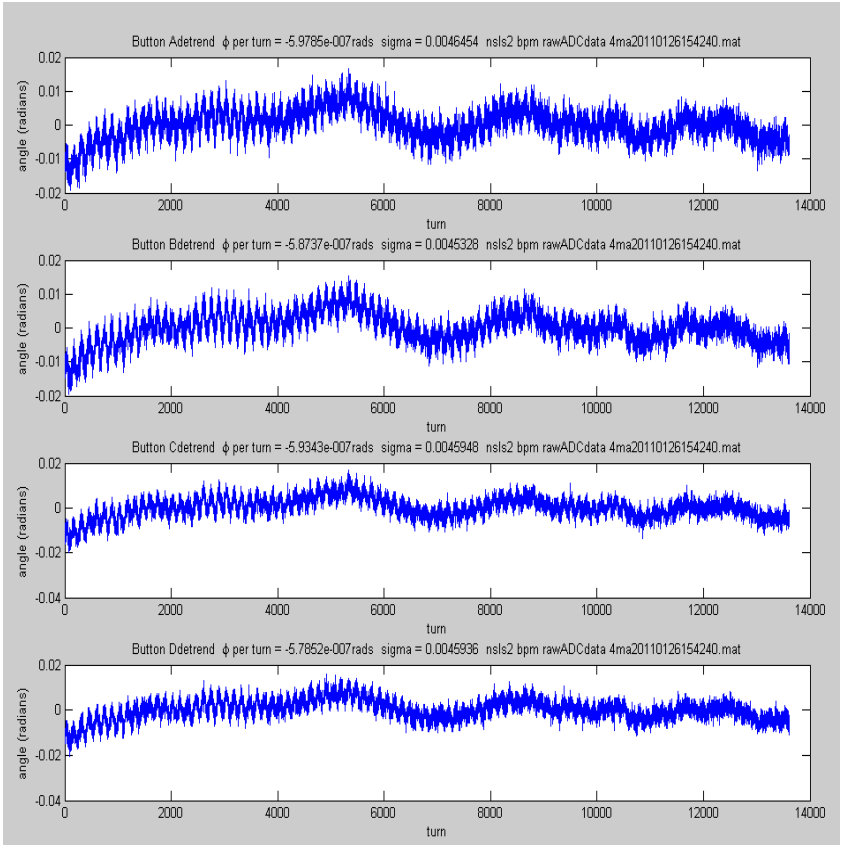
Note: For 25mm aperture 0.3/1000 ~ 8um (electronics performance)

ALS Single-Bunch Performance

4ma (2.6nC) Single Bunch – 77 Samples/Turn @ Trev=656ns



Button Amplitude Response

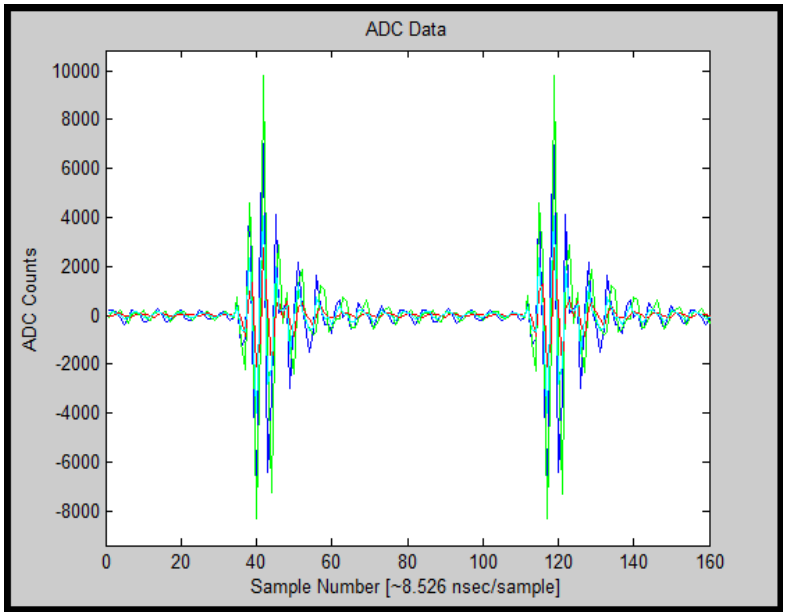


Button Phase Response

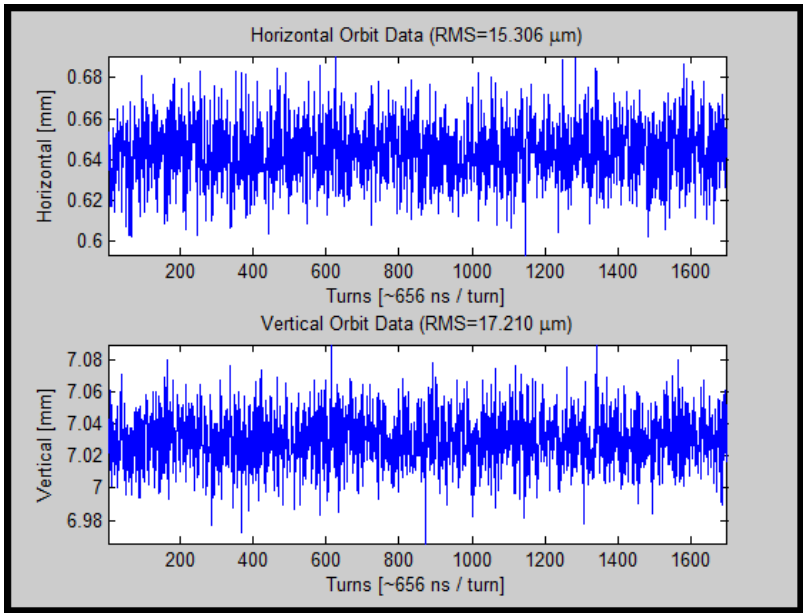
Analysis performed on 1M raw ADC Samples. Complex Translation of Digital IF (h=20) to Baseband. Correlates to Internal TbT Calculation

ALS Single-Bunch Measurements

2-4mA Single Bunch in Bucket 318 (2/15/11)



Single bunch ADC data at ~3 mA



Computed orbits

10dB of attenuation between BPM Electronics and Pickup

ALS TbT Analysis

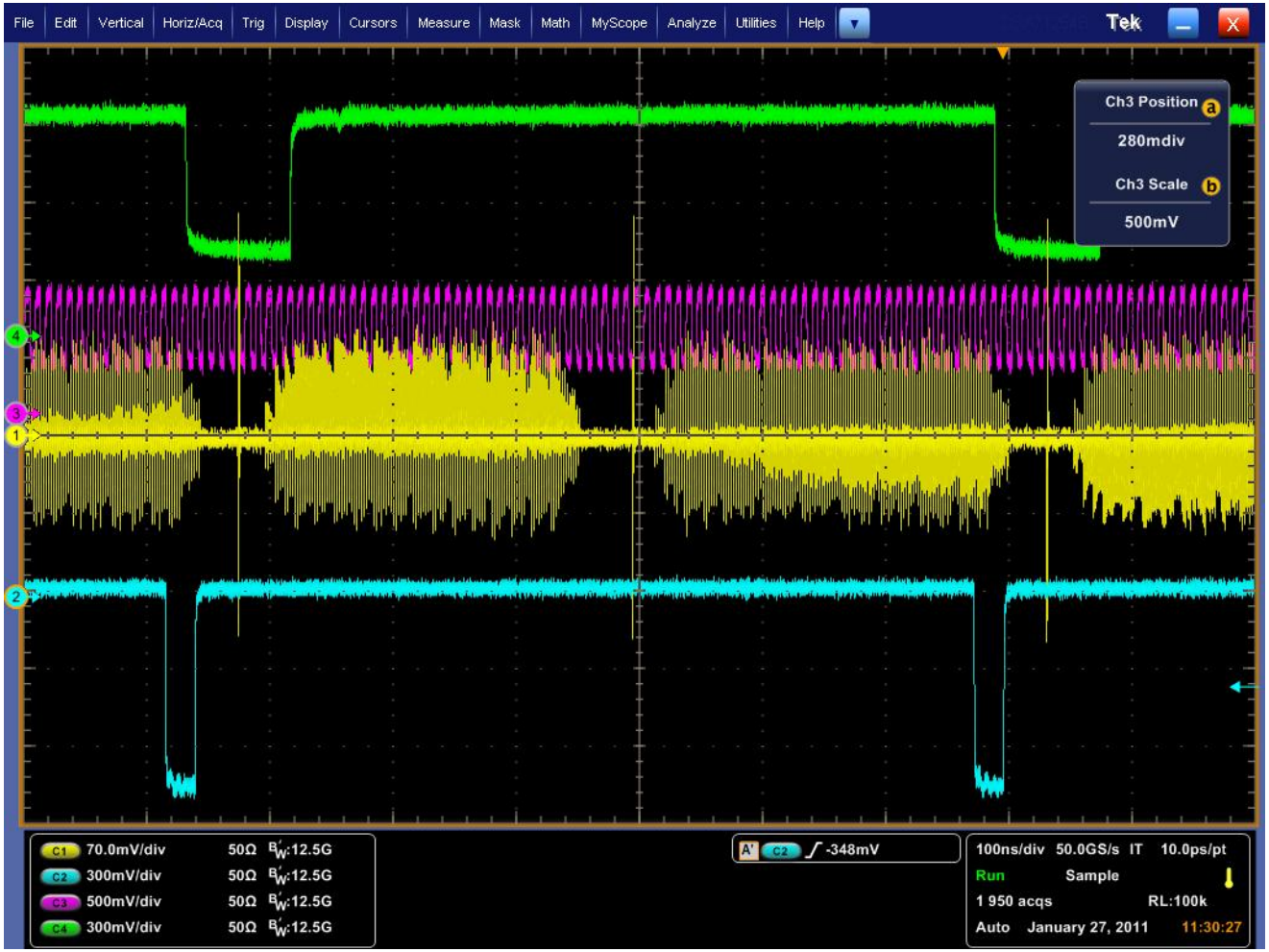
500 mA, user operations, top-off, double-cam fill pattern

Processing Gate

ADC Clock

Beam

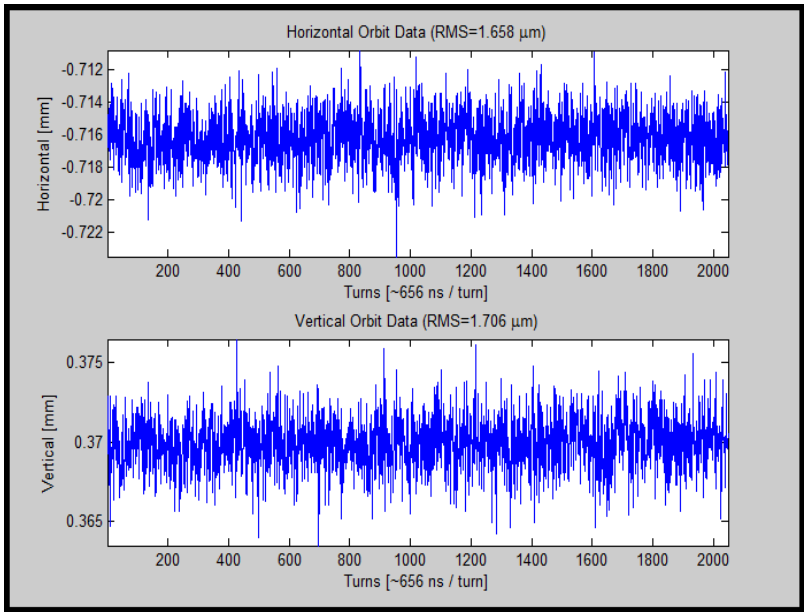
Machine Clock (Frev)



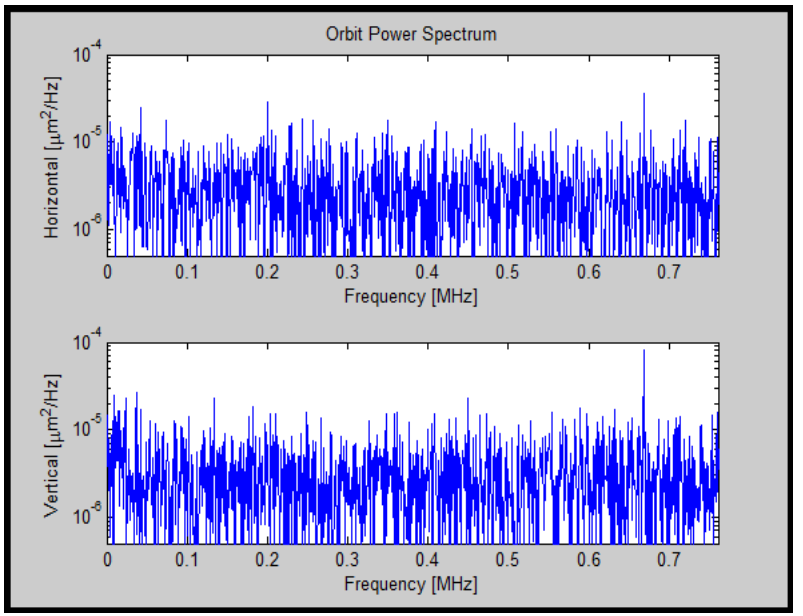
Timing Setup Prior to taking data

ALS TbT Analysis

500 mA, user operations, top-off, double-cam fill pattern

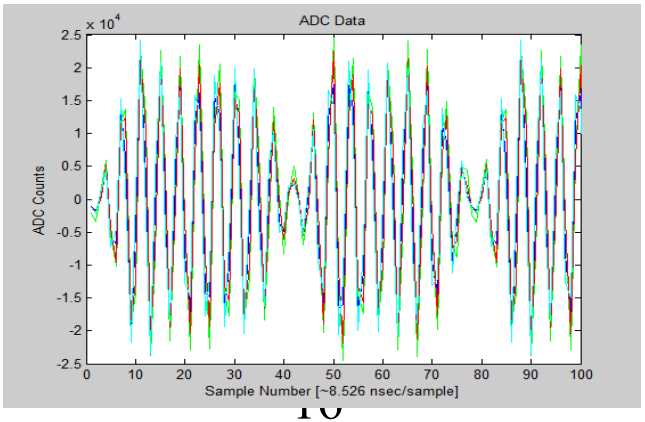


Position calculation using only the "500 MHz" DFT bin. The geometric gain is 16.13 horizontally and 16.29 vertically.



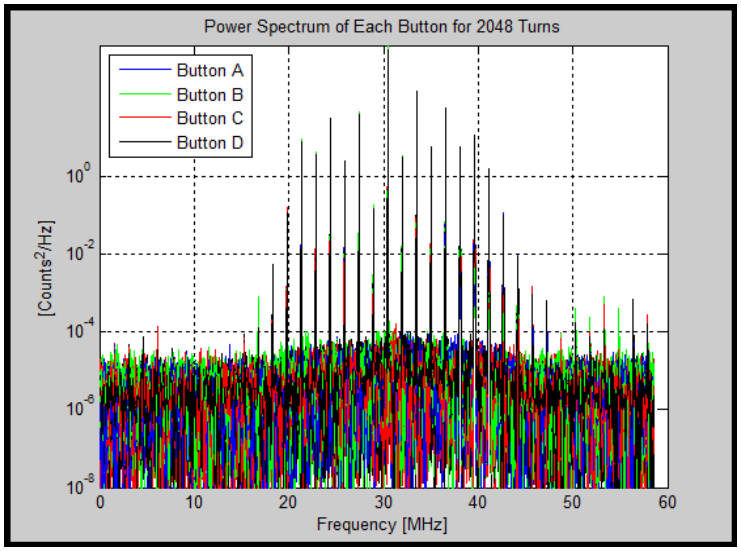
Orbit Power Spectrum

ADC Data 4-button overlay

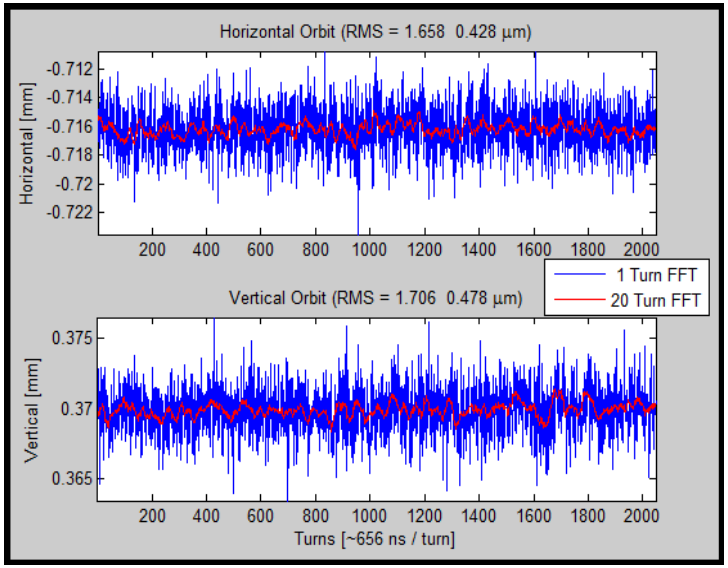


Single Turn & 20-Turn Comparison

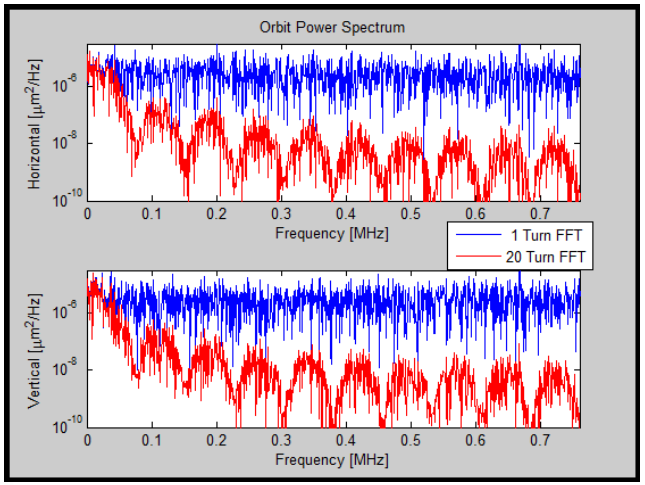
500 mA, user operations, top-off, double-cam fill pattern



20-Turn Power spectrum

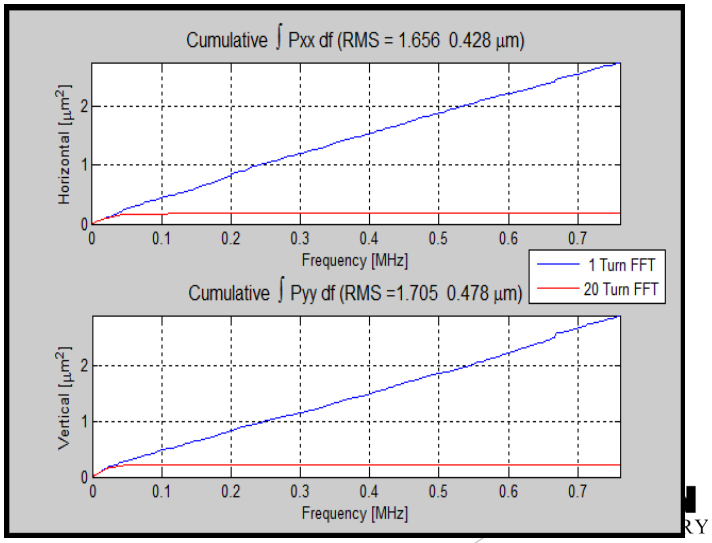


Time series orbit calculation comparison for 1 and 20 turn DFTs.



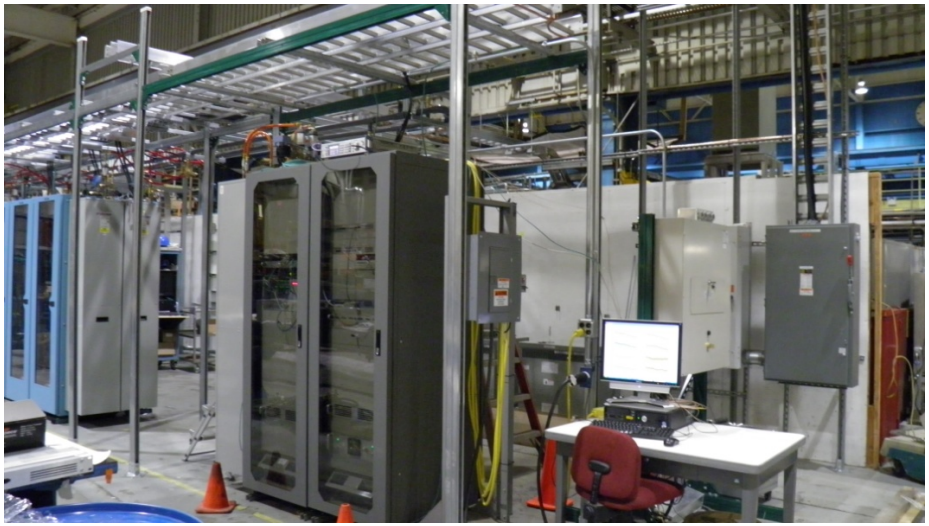
PSD Orbit Calculation comparison for 1 and 20-turn FFT

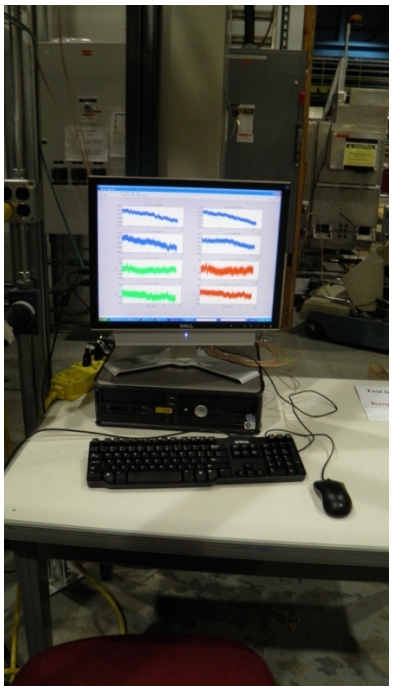
"The ALS specification of about .5 µm rms is already met. ***Further down sampling of the orbit to 10 kHz with a block average reduced the rms by a factor of 2.5 to .17 µm horizontally and .18 µm vertically" (ALS)***



Long-Term Stability Testing

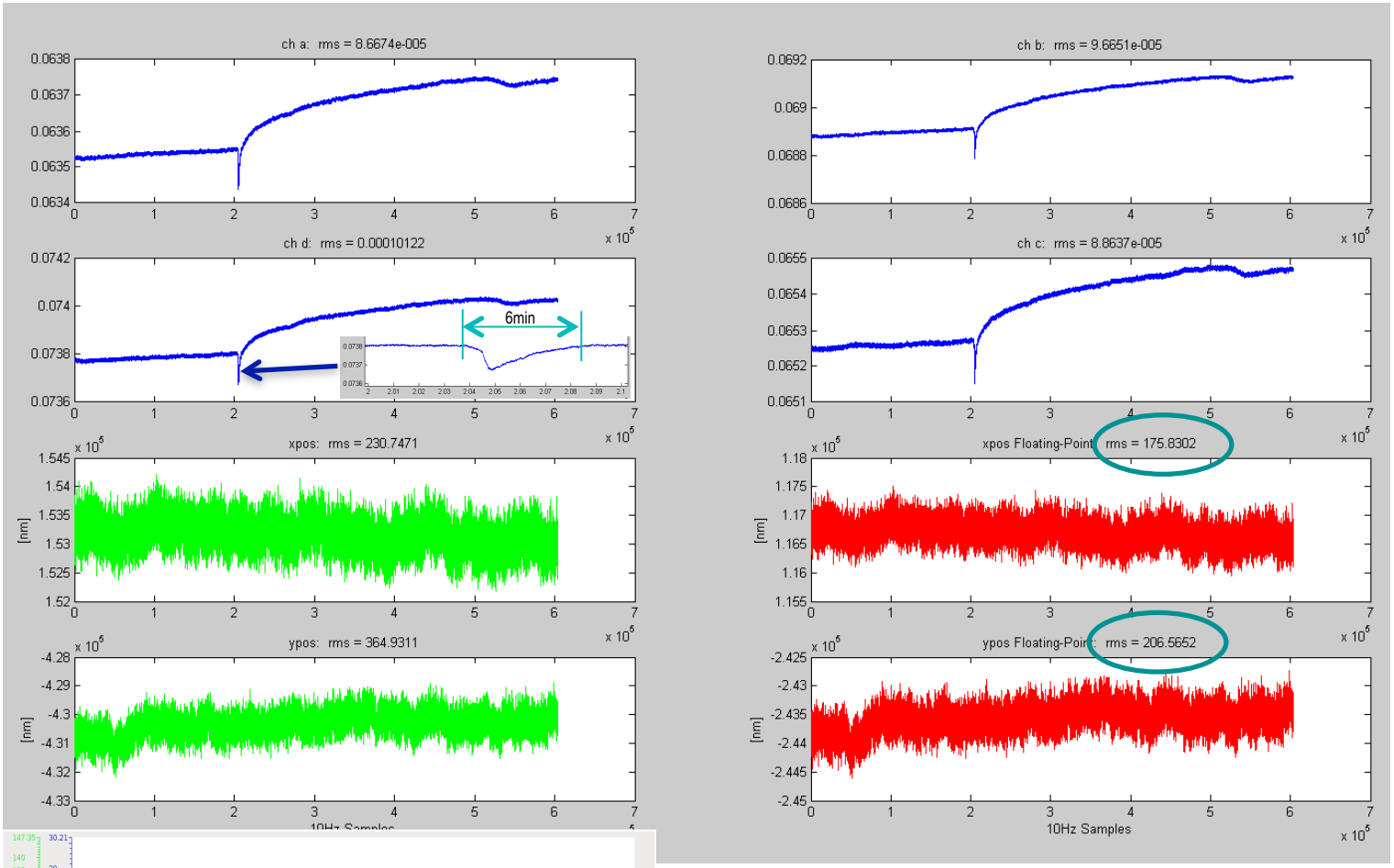
- Currently quantifying thermal effects on BPM system in NSLS-II BPM +/- 0.1C rack located in basement of 902
- Experiments run thus far:
  - BPM in rack with short cable to 4-way splitter
  - BPM in rack, 50ft of LMR240 outside rack
- No dynamic calibration (i.e. Pilot-Tone not implemented)
- RF Configuration
  - R&S SMA100 external to rack @ -30dBm, CW
  - Power Splitter (1:4) and short cables inside rack

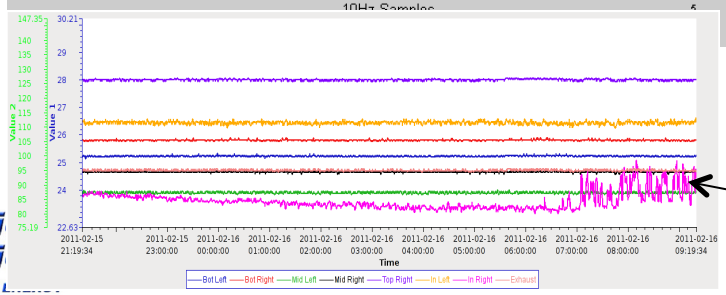




Overnight Stability Test – 16.7hrs

2/15 (4:21pm) to 2/16 (9:48am)





12hr thermal data starting at 9:19pm on 2/15

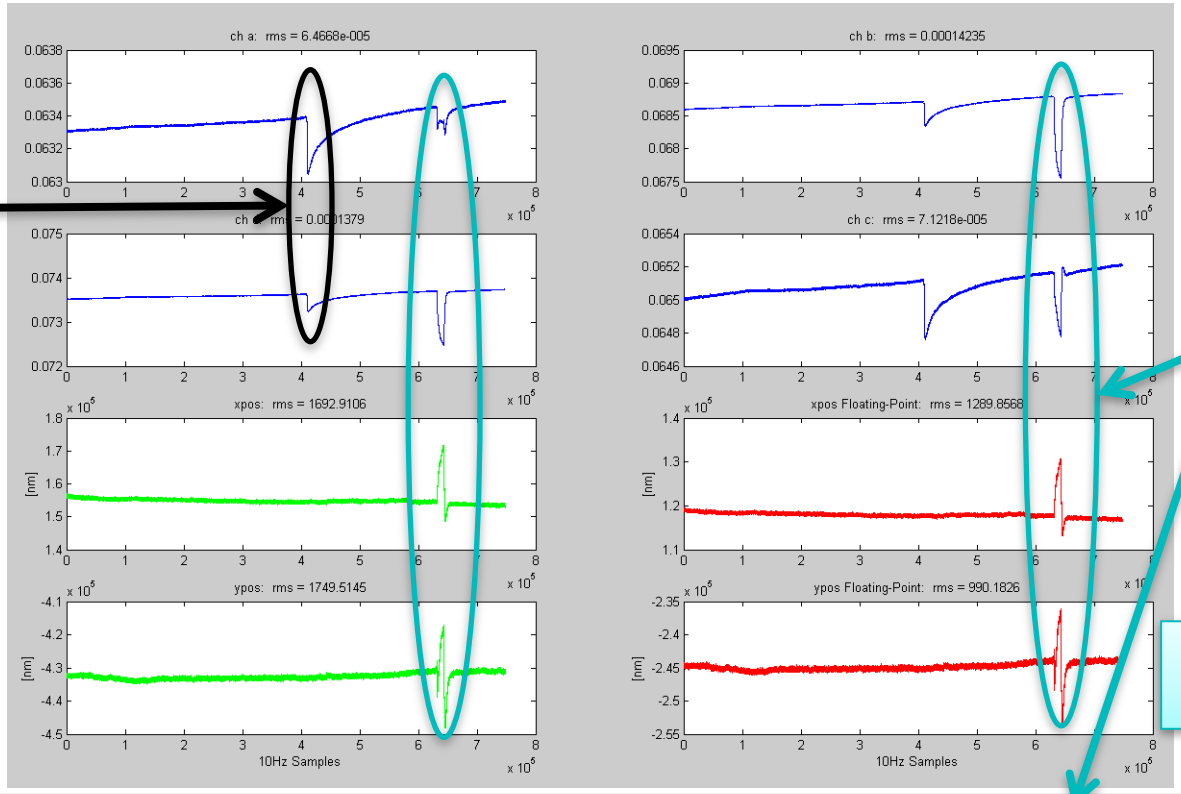
Ambient

Overnight Stability Test – 21hrs

2/14 (4pm) - 2/15 (1:37pm), Open BPM Rack Doors for ½ hr

Unknown Perturbation on all 4-channels.

Most likely related to signal generator since there was no change in X or Y position

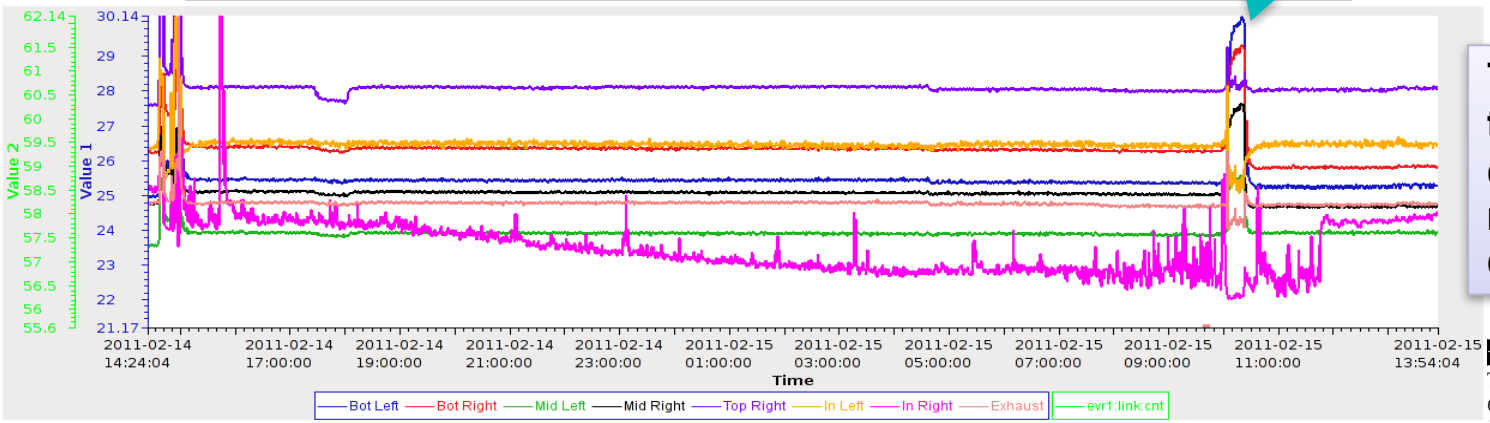


Doors opened from 9:58am - 10:23am

Time	Chassis Internal Temp. (°C)
9:50	25.30
10:22	41.00
10:34	25.80
11:30	25.23

Position change(T) ~ 15um(pp)

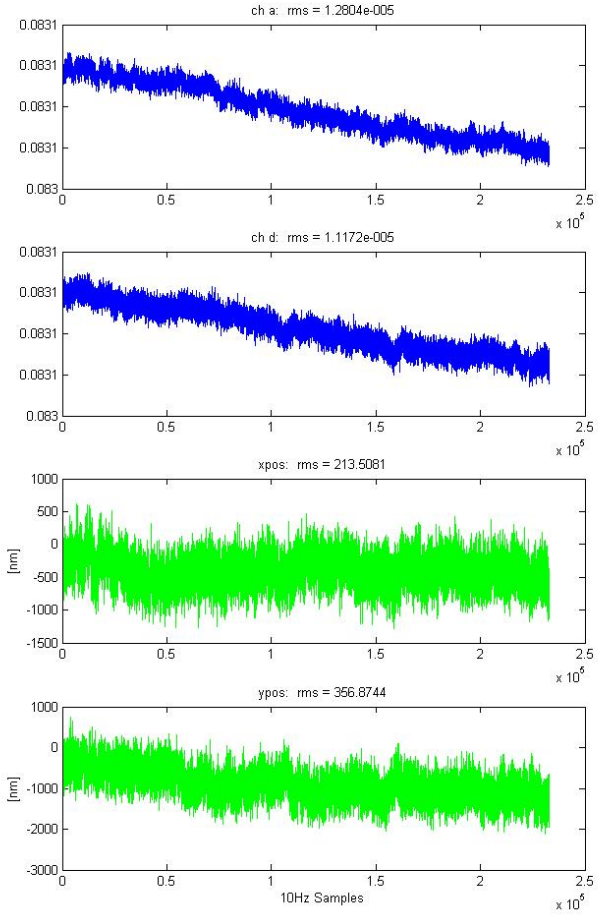
ΔT = 15.7°C

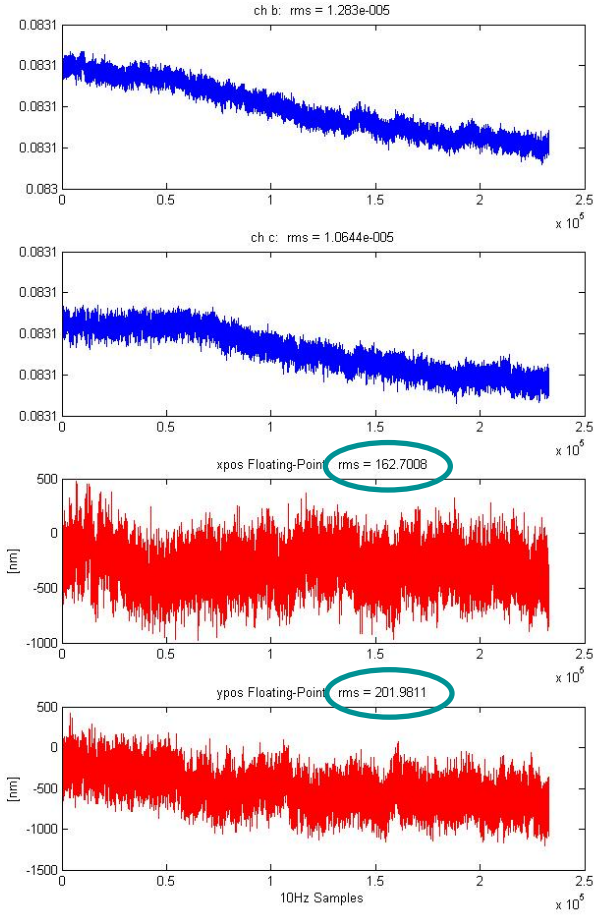


Thermal Plot time -scale does NOT match BPM data

External Cable Test (6.5hrs)

50ft LMR240 Located Outside of Rack (10am – 4:30pm, 2/17/11)





No performance change with cables outside rack during 6.5hr daytime run

Summary

- Built and tested 10 DFE's (1st spin)
- Built and tested 4 AFE's (2nd spin)
- Installed two units at ALS
- Successfully ported Virtex-5 design to Virtex-6
- Virtex-6 transitional test platform working
- Successfully implemented TCP/IP EPICS communication
- Successfully implemented TCP/IP MatLab communication
- Long-Term testing suggests 200nm 8hr+ stability can be achieved
- AFE Spin-2 (clean-up) in fabrication
- DFE Spin-2 (Virtex-6) near completion, Lab testing in March
- Performed beam test at ALS (on-going effort)
- Conducted Pilot-Tone studies at ALS

ERL Enabling Technologies

ANALOG DEVICES

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

AD9467

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM

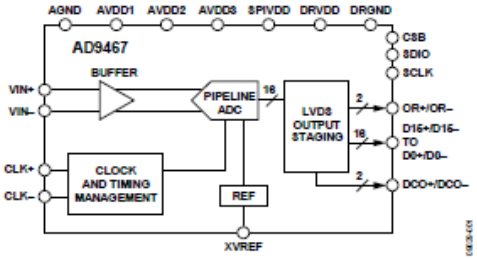


Figure 1.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

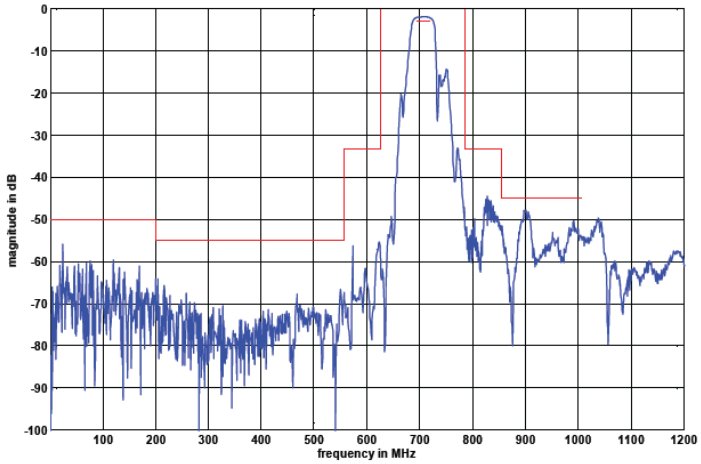
Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

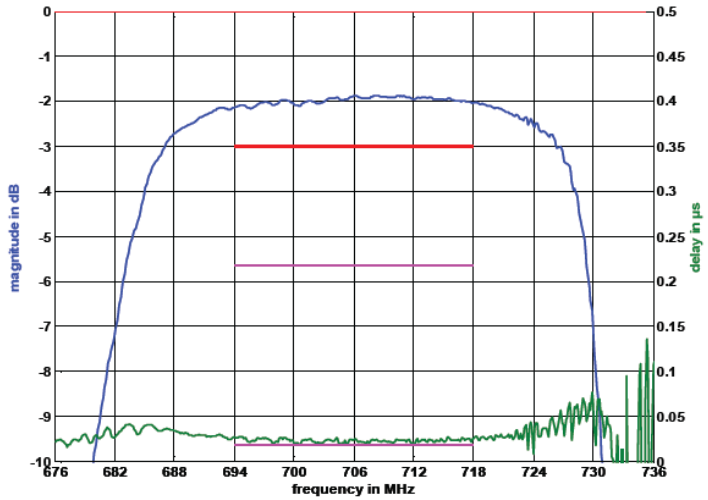
The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. IF optimization capability used to improve SFDR.
2. Outstanding SFDR performance for IF sampling applications such as multicarrier, multimode 3G, and 4G cellular base station receivers.

700MHz SAW Filter





Analog BW = 900MHz

NSLS-II has AD9467 in BPM lab

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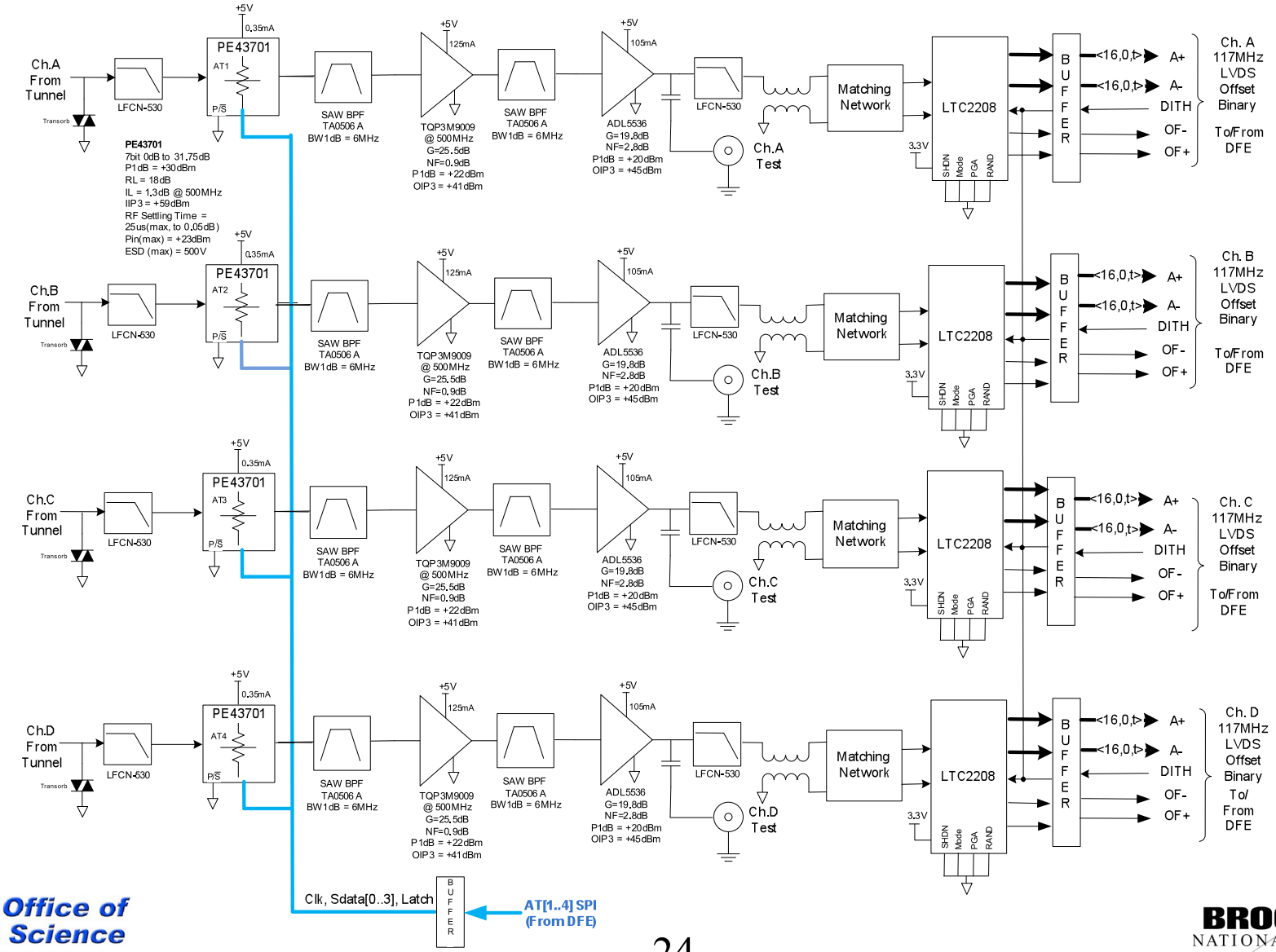
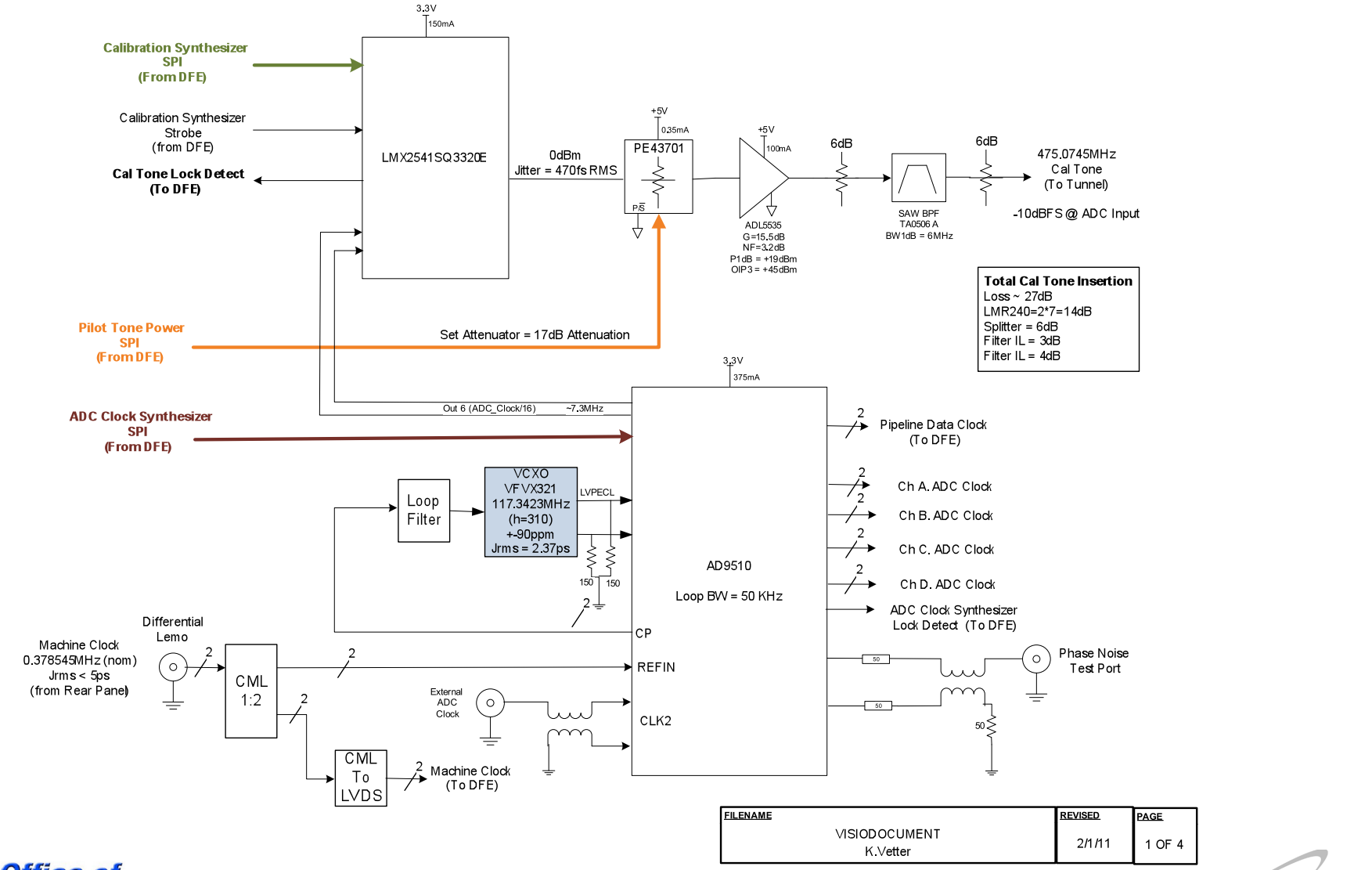
System Architecture – AFE Receiver

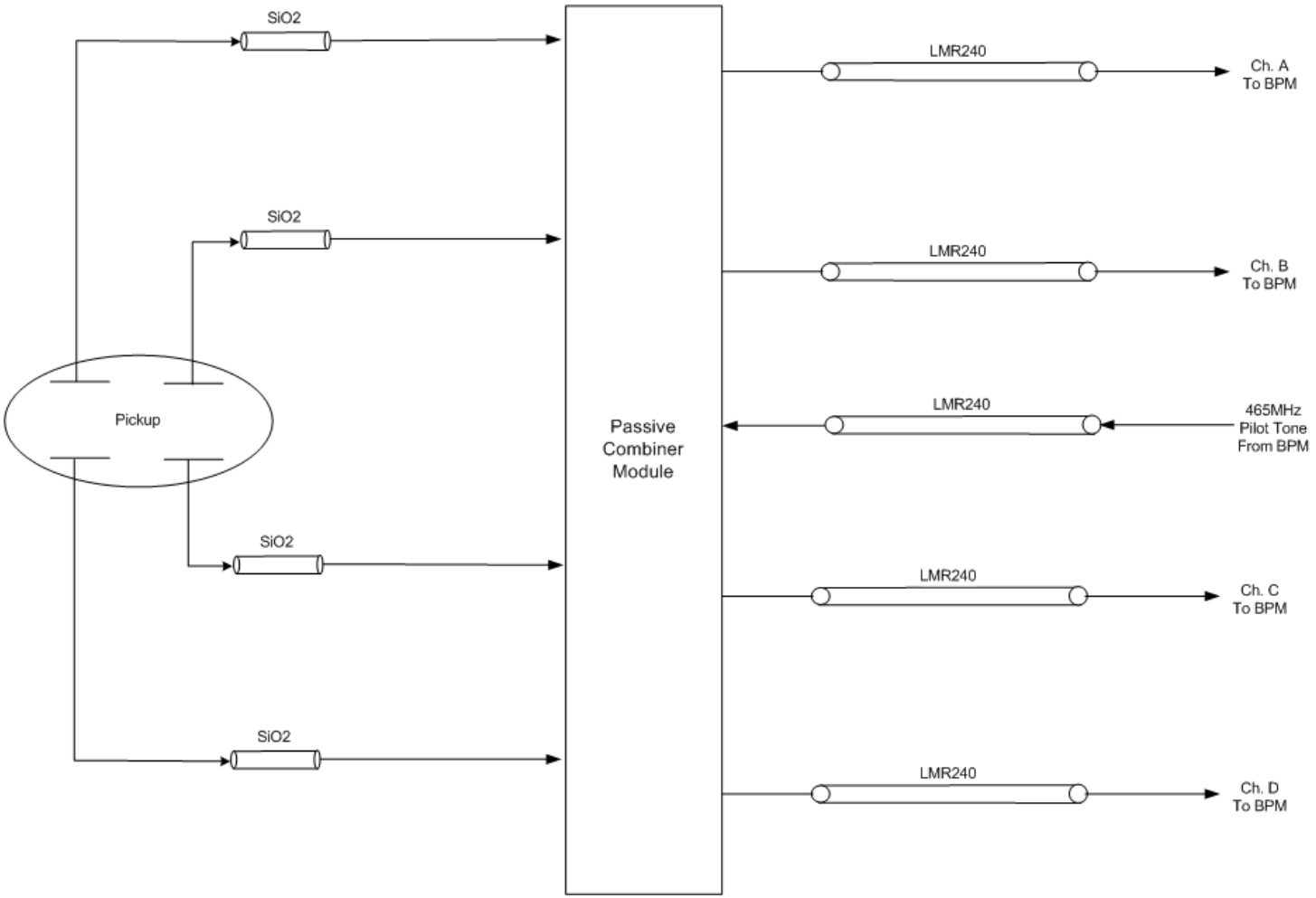


System Architecture – AFE Synthesizer

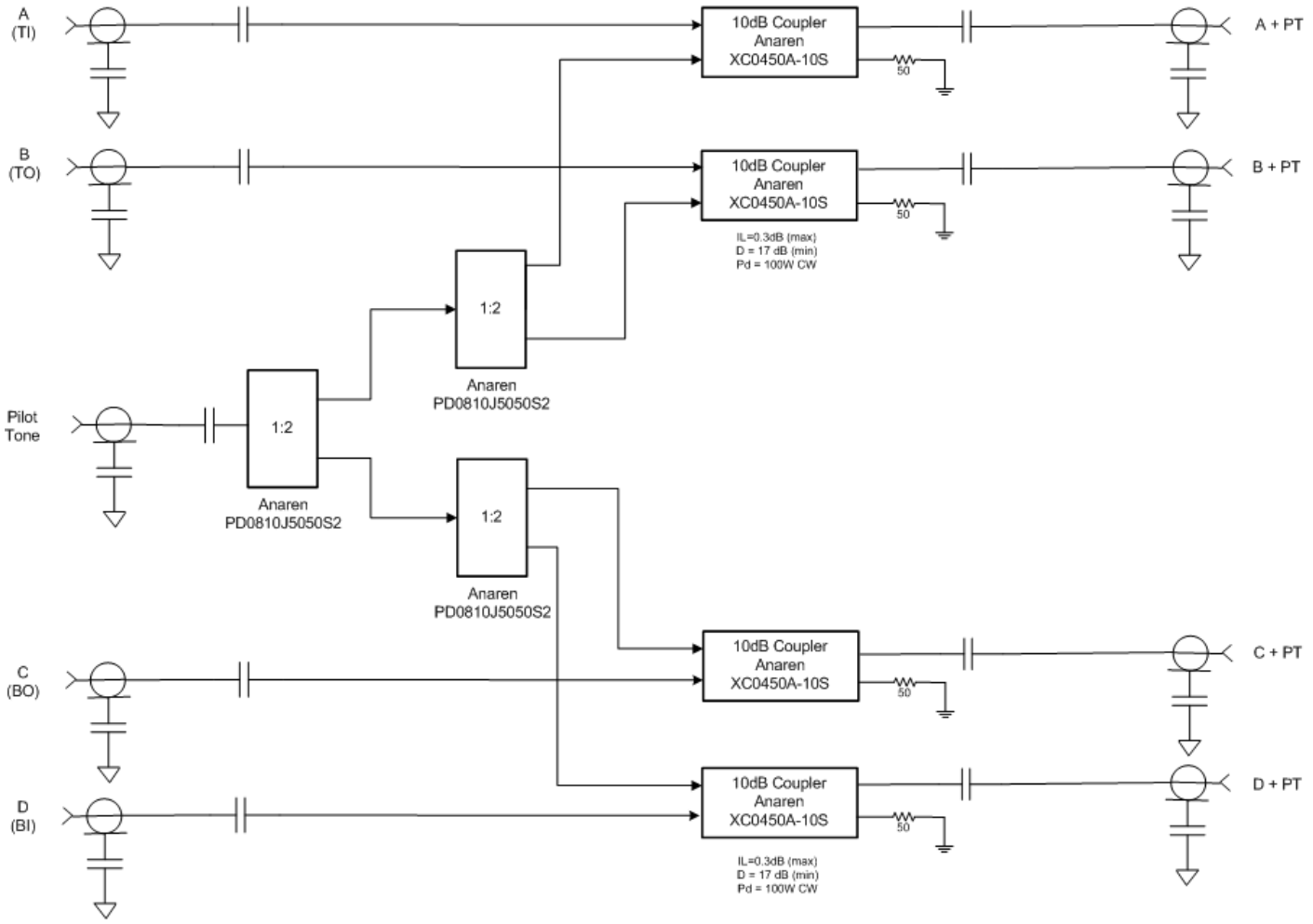


Backup Slides

Pilot-Tone Combiner – Tunnel Configuration



Passive Pilot-Tone Combiner



Injector RF BPM Resolution Requirement – Single shot

Parameters/ Subsystems	Conditions	Vertical	Horizontal
Injector single bunch single shot	0.05 nC charge	300 μm rms	300 μm rms
	0.50 nC charge	30 μm rms	30 μm rms
Injector multi bunch single shot (80-150 bunches;)	15 nC charge	10 μm rms	10 μm rms

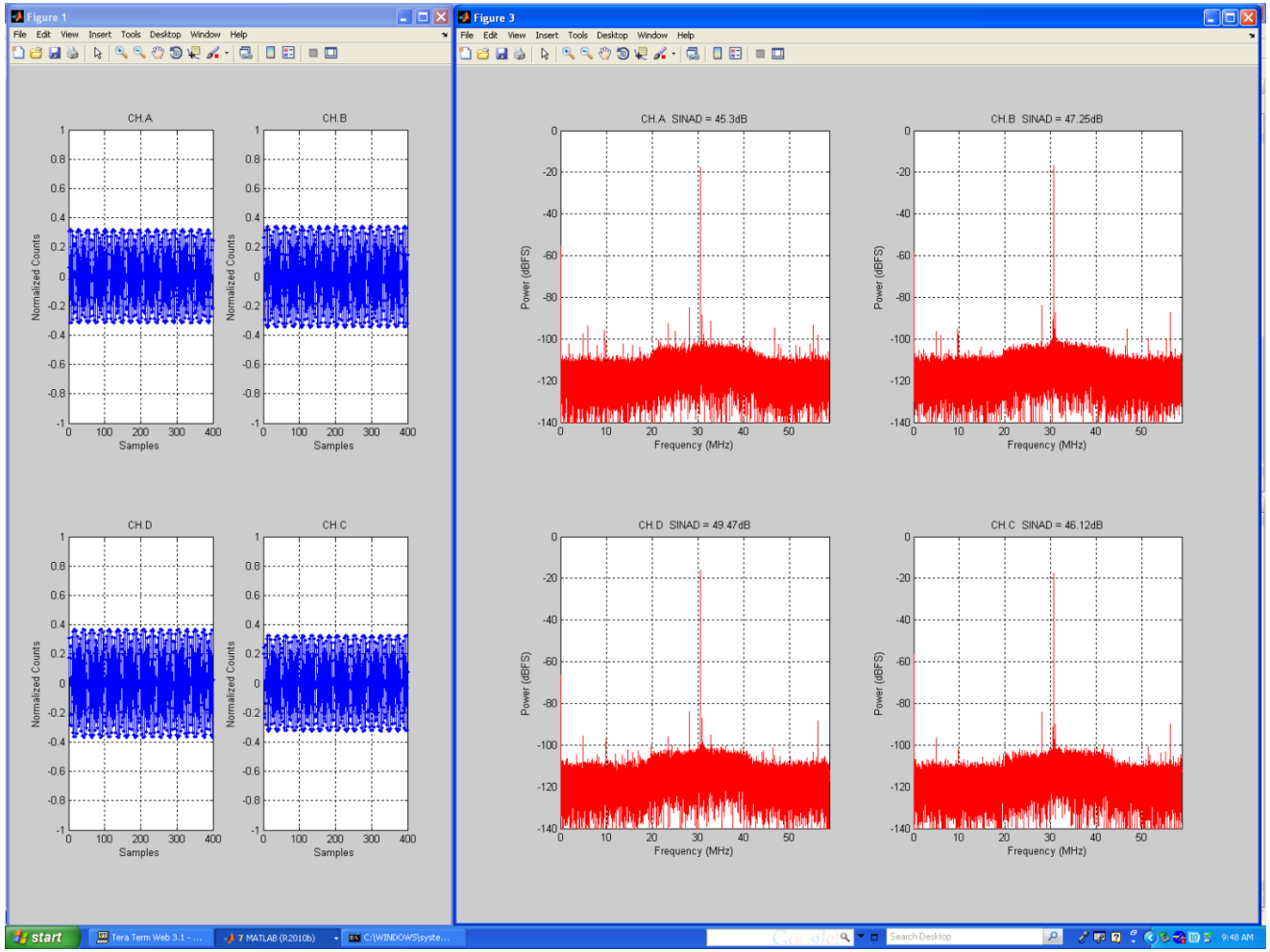
- Linac rep rate = 10 Hz;
- Booster ramp rate = 1 Hz;
- Booster revolution frequency = 1.98 MHz;
- Storage ring revolution frequency = 378 kHz;
- Bunch spacing = ~ 2ns
- Bunch length = 15 – 30 ps

SR RF BPM Resolution Requirement – Stored beam

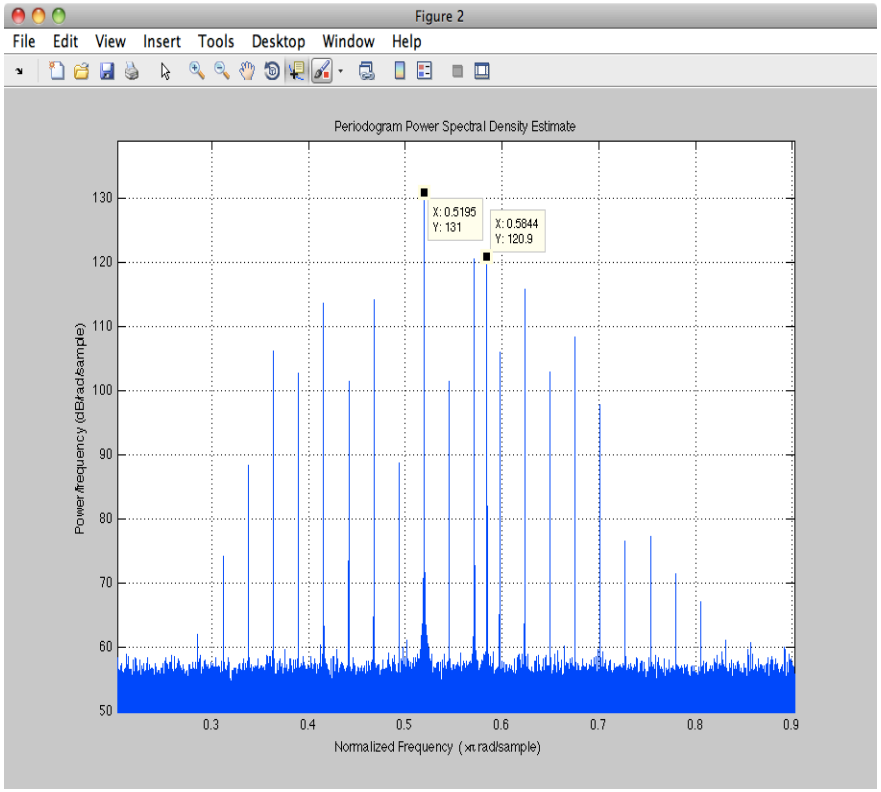
Parameters/ Subsystems				Conditions	*Multipole chamber RF BPM Resolution Requirement	
					Vertical	Horizontal
50 mA to 500 mA Stored beam resolution – 20% to 100 % duty cycle	BPM Receiver Electronics	Turn by Turn (80% fill)		Data rate = 378 kHz	3 μm rms	5 μm rms
		Assuming no contribution from bunch/ fill pattern effects		0.017 Hz to 200 Hz	0.2 μm rms	0.3 μm rms
				200 Hz to 2000 Hz	0.4 μm rms	0.6 μm rms
				1 min to 8 hr drift	0.2 μm peak	0.5 μm peak
		Bunch charge/ fill pattern effects only		DC to 2000 Hz	0.2 μm rms	0.3 μm rms
	Mechanical motion limit at Pick-up electrodes assembly (ground & support combined)		Vibrations	50 Hz to 2000 Hz	10 nm rms	10 nm rms
				4 Hz to 50 Hz	25 nm rms	25 nm rms
				0.5 Hz to 4 Hz	200 nm rms	200 nm rms
			Thermal	1 min to 8 hr	200 nm peak	500 nm peak

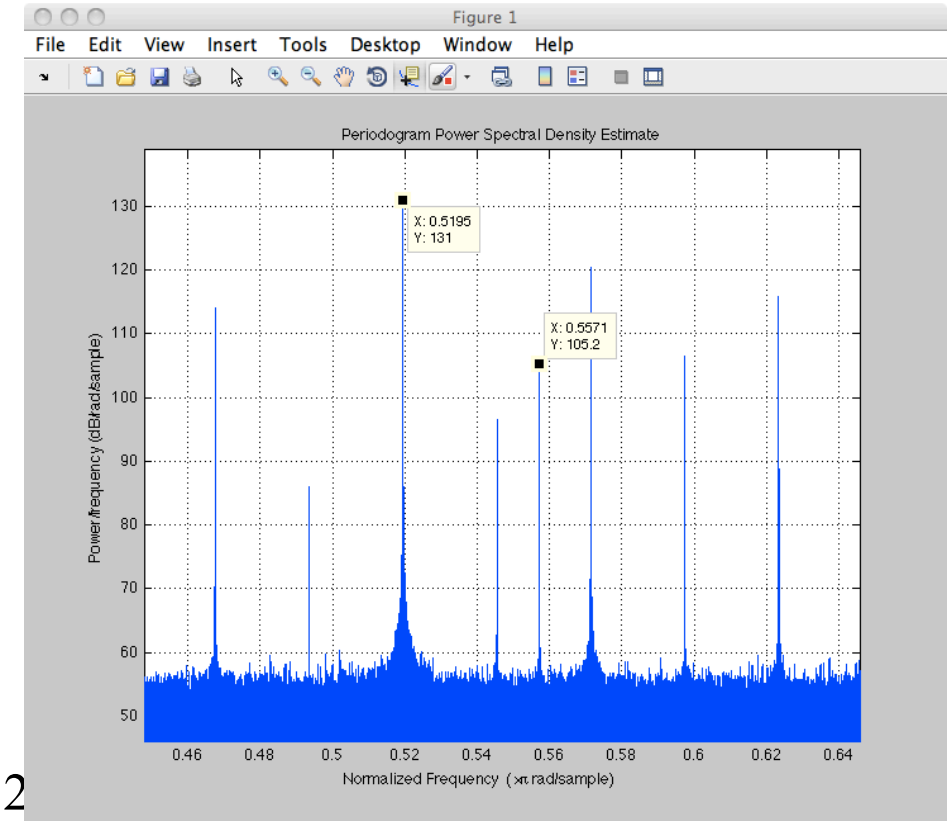
*ID straight section RF BPM requirements to be better

Long-Term Stability Time/Frequency Test



ALS Pilot-Tone Study





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BPM Material Cost

- AFE = $1,300
- DFE = $1,700
- Chassis = $300
- Combiner = TBD
- Assembly = TBD

Note: AFE and DFE cost in based on 10pc quantity

ERL Sampling Numerology

ERL Numerology		
Parameter	**SR**	**Units**
RF Frequency	703.7500	MHz
Harmonic	75.02665245	
Revolution Frequency	9.380000	Mhz
Revoluton Period	1.066E-07	sec
ADC Clock Harmonic	18	
ADC Clock	168.8400	MHz
ADC Mixing Harmonic	4	
n*fs	675.3600	
DDC Harmonic	3	
Digital IF Frequency	**28.39**	Hz